

**AMENDMENT AND RESPONSE****PAGE 2**

Serial No.: 10/811,617

Attorney Docket No. 125.013US03

Filing Date: March 29, 2004

Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC  
GETTERING ZONE**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of claims:**

1. (Original) A method of forming a semiconductor device comprising:  
implanting ions through a first surface of a monocrystalline semiconductor material to a selected depth forming an amorphous layer adjacent the first surface;  
heating the semiconductor material to convert the amorphous layer to a first layer of semiconductor material; and  
bonding a handle wafer to the first surface of the semiconductor material.
2. (Original) The method of claim 1, further comprising:  
heating the semiconductor material under conditions effective to coalesce a substantially planer zone formed by the implantation of ions through the first surface of the semiconductor material to form a gettering zone.
3. (Original) The method of claim 1, wherein bonding the handle wafer to the first surface of the semiconductor material further comprises:  
forming an insulating bond layer on a surface of the handle wafer; and  
bonding the insulating bond layer to the first surface of the semiconductor material.
4. (Original) The method of claim 1, wherein implanting ions through a first surface of the monocrystalline semiconductor material to a selected depth further comprises:  
implanting ions of the semiconductor material.
5. (Original) The method of claim 1, wherein implanting ions through a first surface of the monocrystalline semiconductor material to a selected depth further comprises:

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implanting silicon ions.

6. (Original) The method of claim 1, further comprising:

forming devices in a second layer of semiconductor material to form an integrated circuit, wherein the second layer of semiconductor material has not been exposed to ion implantation.

7. (Original) The method of claim 1, further comprising:

forming at least one device in a second layer of semiconductor material, wherein the second layer of semiconductor material has not been exposed to ion implantation.

8. (Original) The method of claim 7, wherein the at least one device is a device from a group of devices consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor and a thyristor.

9. (Original) The method of forming an integrated circuit in a wafer of semiconductor material, the method comprising:

implanting ions through a first surface of the wafer to form a first amorphous layer adjacent the first surface of the wafer;

annealing the wafer to convert the first amorphous layer to a first monocrystalline semiconductor layer;

bonding a handle wafer to the first surface of the wafer; and

forming semiconductor devices in a second layer of the wafer adjacent a second surface of the wafer, wherein the second layer has not been exposed to the ion implantation.

10. (Original) The method of claim 9, wherein annealing the wafer to convert the first surface of the wafer comprises:

heating the wafer from 450° C to 1200° for about 15 minutes to 8 hours.

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11. (Original) The method of claim 9, wherein implanting the ions to form the first amorphous layer further comprises:

implanting ions of the semiconductor material of the wafer to form the first amorphous layer.

12. (Original) The method of claim 9, wherein bonding the handle wafer to the first surface of the wafer, further comprises:

forming an insulating bond layer on a surface of the handle wafer; and  
bonding the insulating bond layer to the first surface of the wafer.

13. (Original) The method of claim 9, further comprising:

thinning the second layer of the wafer to a desired thickness.

14. (Original) The method of claim 13, wherein the method of thinning the second layer of the wafer to the desired thickness is a method from a group of methods consisting of etching, lapping, grinding and polishing.

15. (Original) The method of claim 9, wherein implanting the ions to form the first amorphous layer further comprises:

forming a oxide layer overlaying the first surface of the wafer; and  
implanting the ions through the oxide layer.

16. (Original) The method of claim 15, further comprising:

removing the oxide layer after the implantation of ions.

17. (Original) The method of claim 9, further comprising:

forming a gettering zone between the first monocrystalline semiconductor layer and the second layer of the wafer.

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18. (Currently amended) The method of claim 17, wherein forming the gettering zone further comprises:

heating the wafer from 88-800° C to 1200° for about 1 to 6 hours.

19. (Original) A method of forming an integrated circuit in a monocrystalline semiconductor wafer, the method comprising:

implanting ions through a first surface of the wafer to form a first layer of amorphous material adjacent the first surface of the wafer which extends a select depth from the first surface; annealing the first layer of amorphous layer to form a first monocrystalline semiconductor layer;

forming a gettering zone containing active gettering sites between the first layer monocrystalline semiconductor material and a second layer of monocrystalline material, wherein the second layer of monocrystalline material has not been exposed to ion implementation;

bonding a handle wafer to the first surface of the wafer; and

forming devices in the second layer of monocrystalline material to form the integrated circuit.

20. (Original) The method of claim 19, wherin implanting the ions to form the first layer of amorphous material a select depth further comprises:

controlling the energy used to implant the ions.